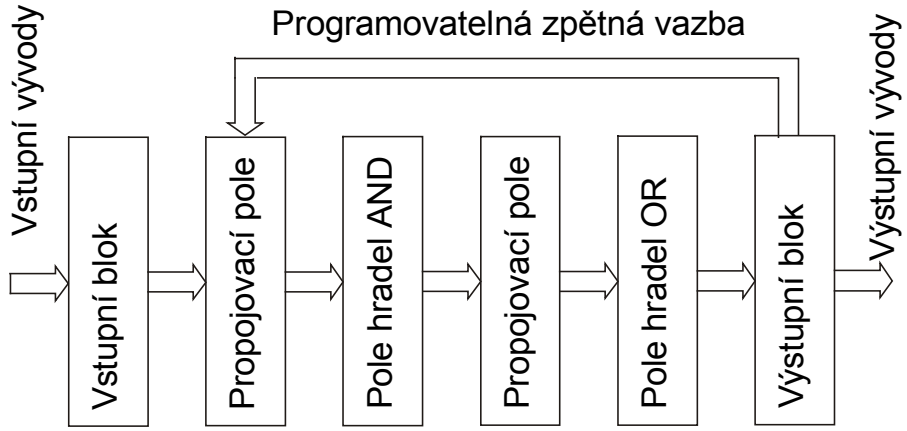
PROGRAMOVATELNÉ LOGICKÉ OBVODY

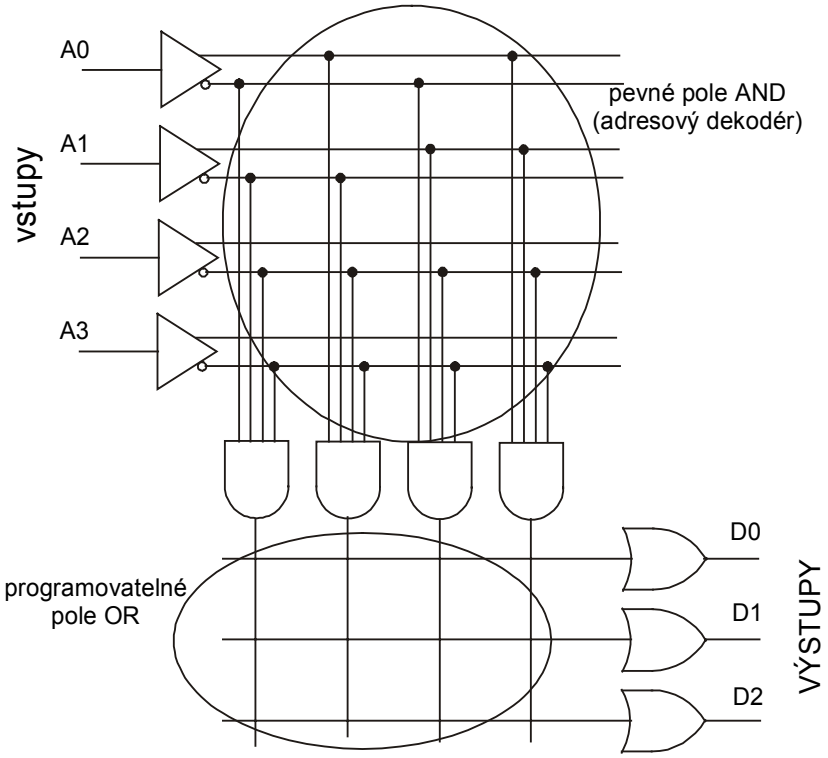
(PROGRAMMABLE LOGIC DEVICE – PLD)

Pozn.: Soubor obsahuje pouze některé obrázky a schémata, která slouží jako podklad pro přednášku k danému tématu.

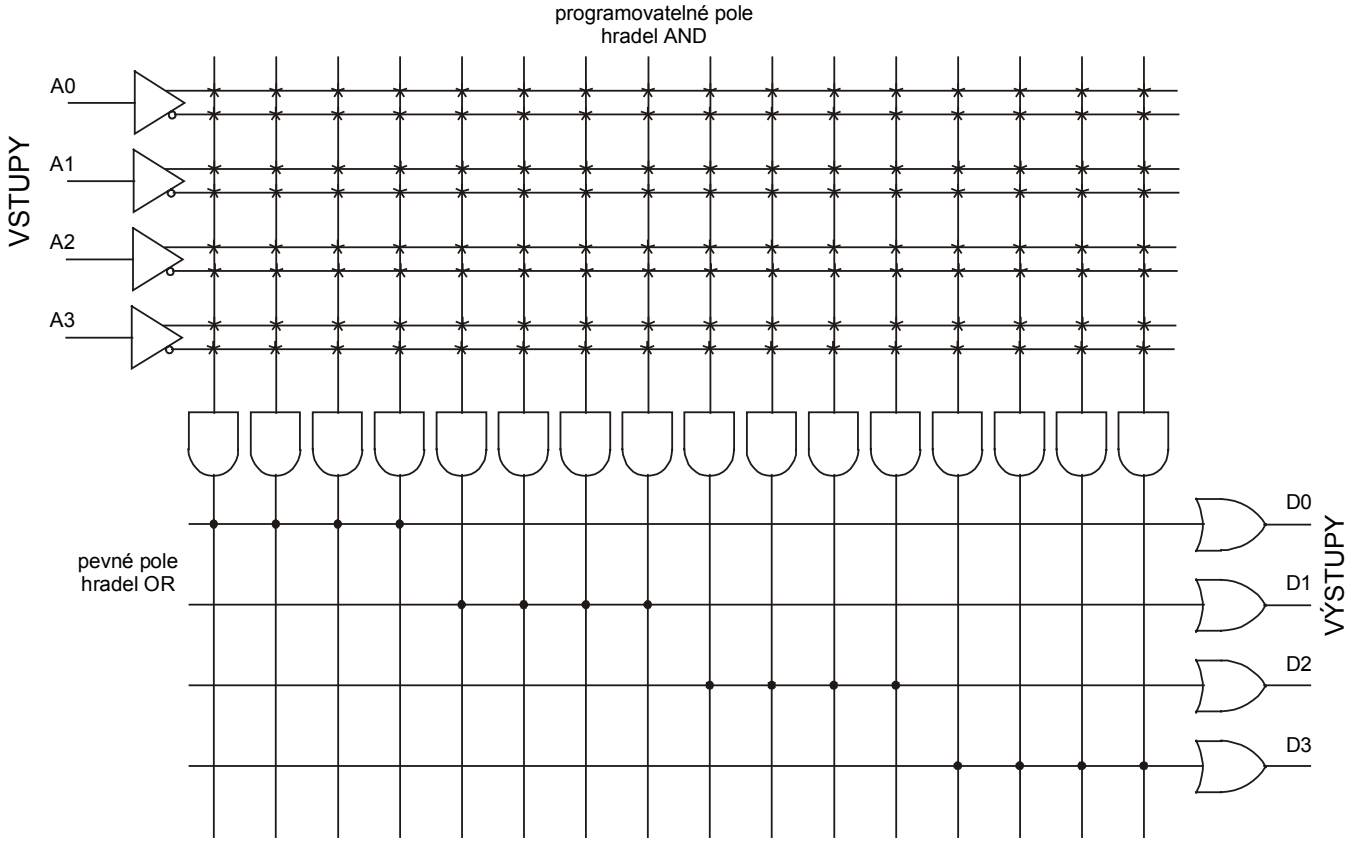


Architektura programovatelného logického pole

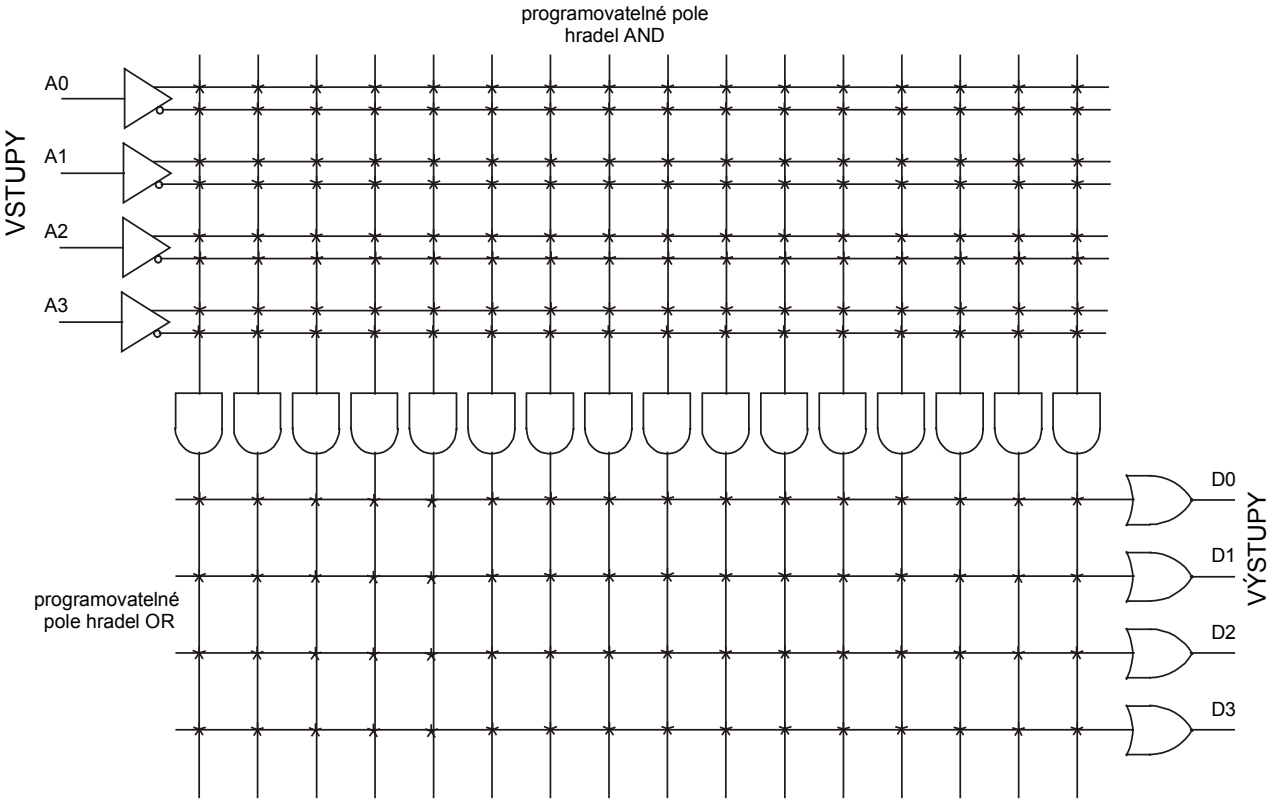
PLD OBVODY TYPU PAMĚTÍ PROM



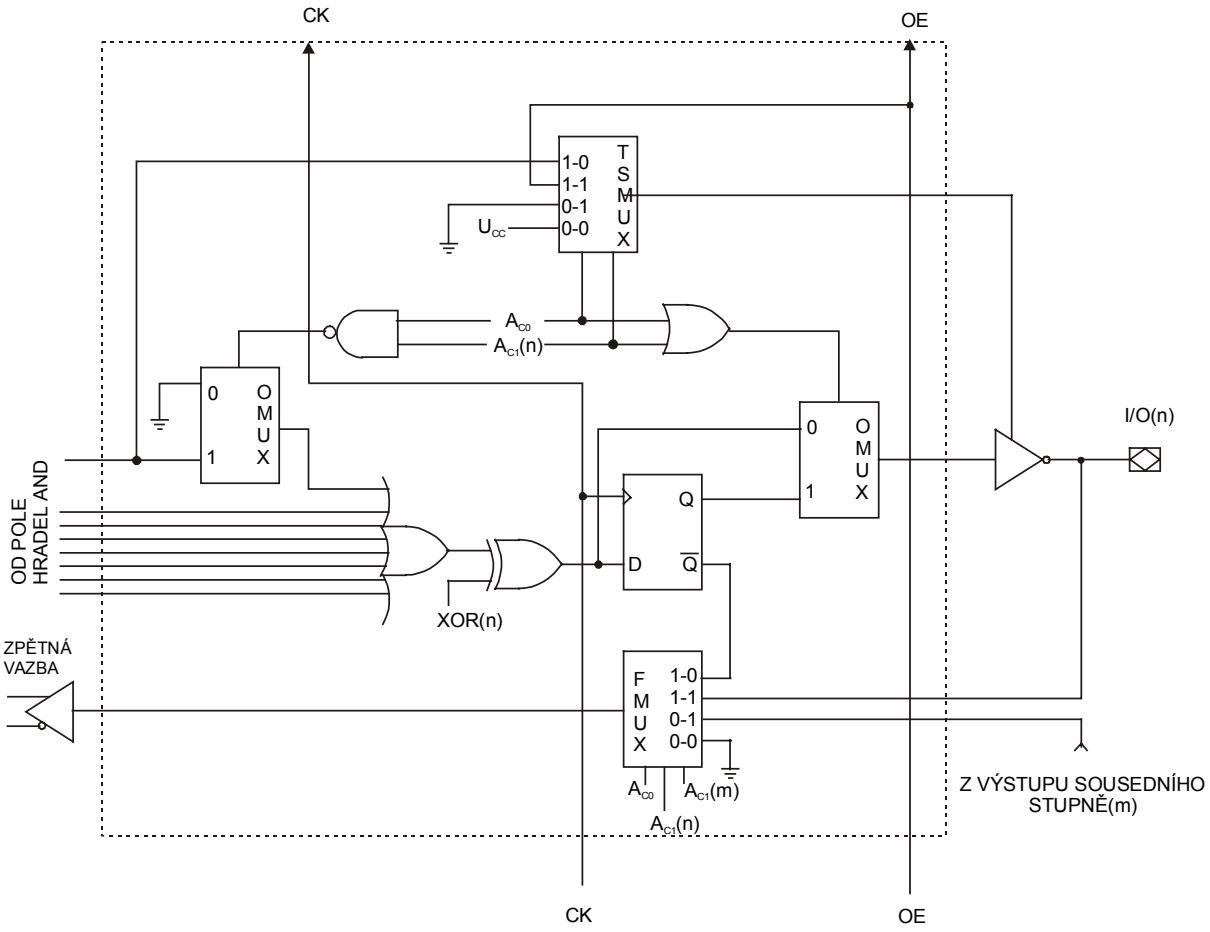
OBVODY PAL (PROGRAMMABLE ARRAY LOGIC)



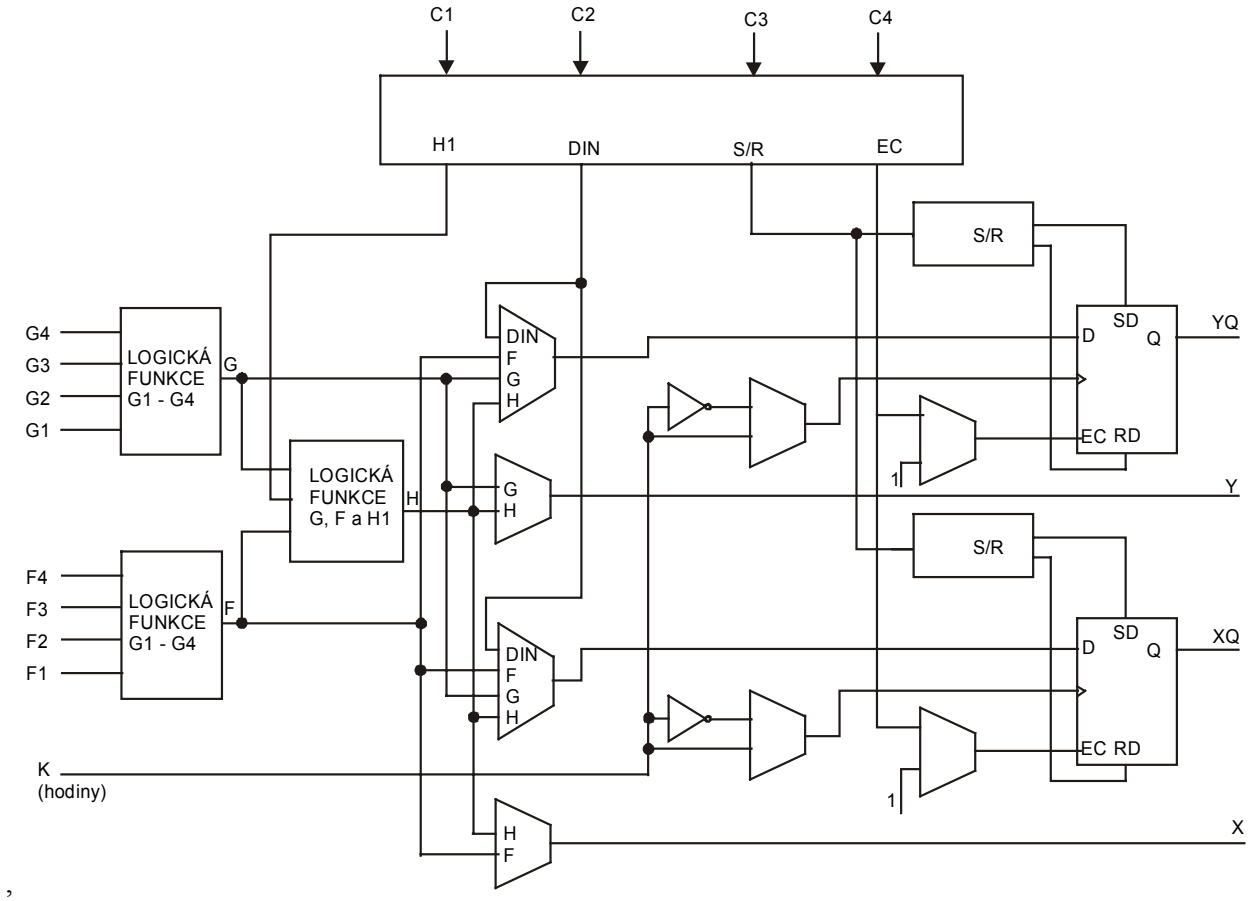
OBVODY FPLA (FIELD PROGRAMABLE LOGIC ARRAY)



OBVODY TYPU GAL (GENERIC ARRAY LOGIC)



OBVODY FPGA (FIELD PROGRAMABLE GATE ARRAY)



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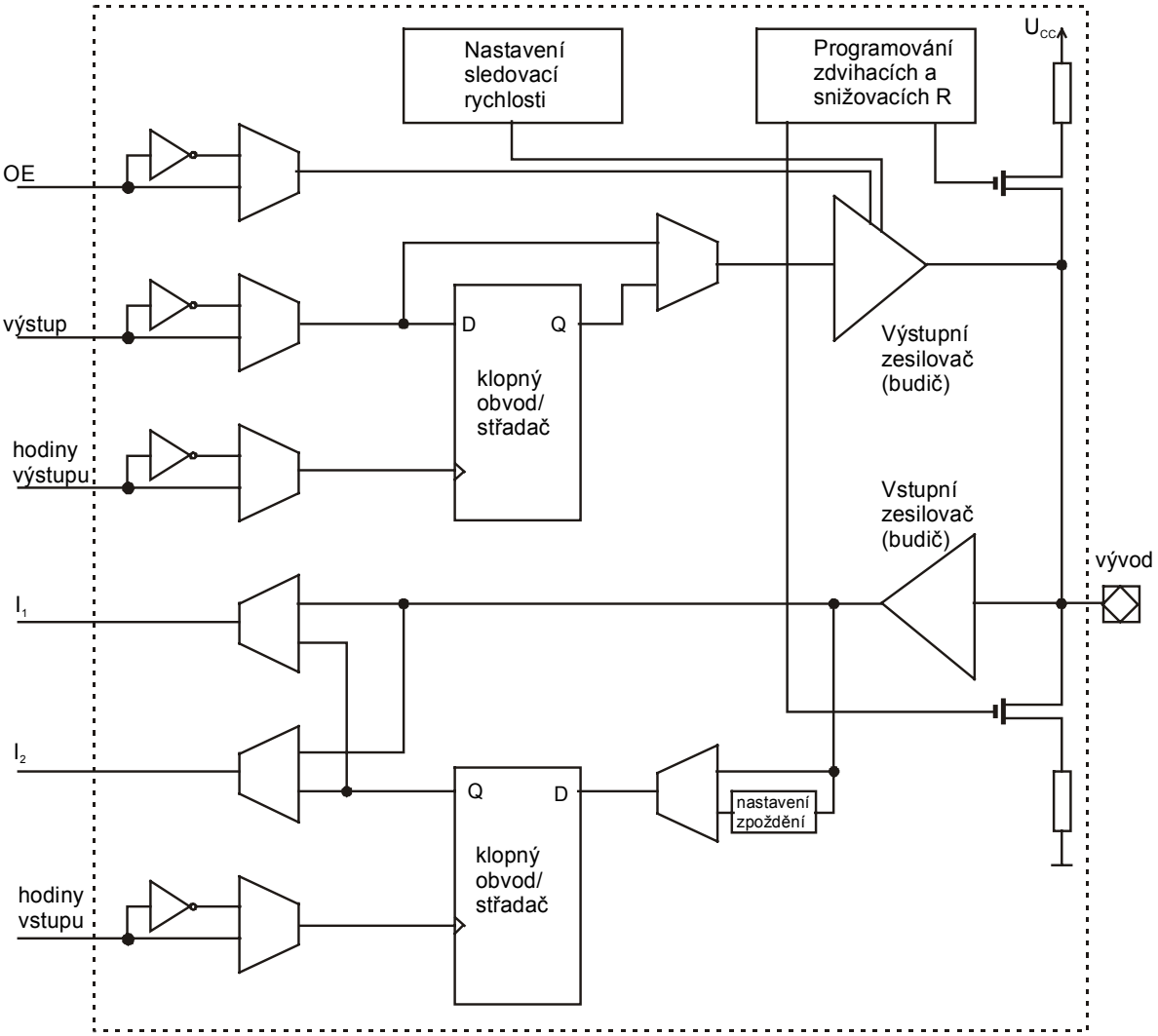
Bloková struktura CLB



Bloková struktura IOB