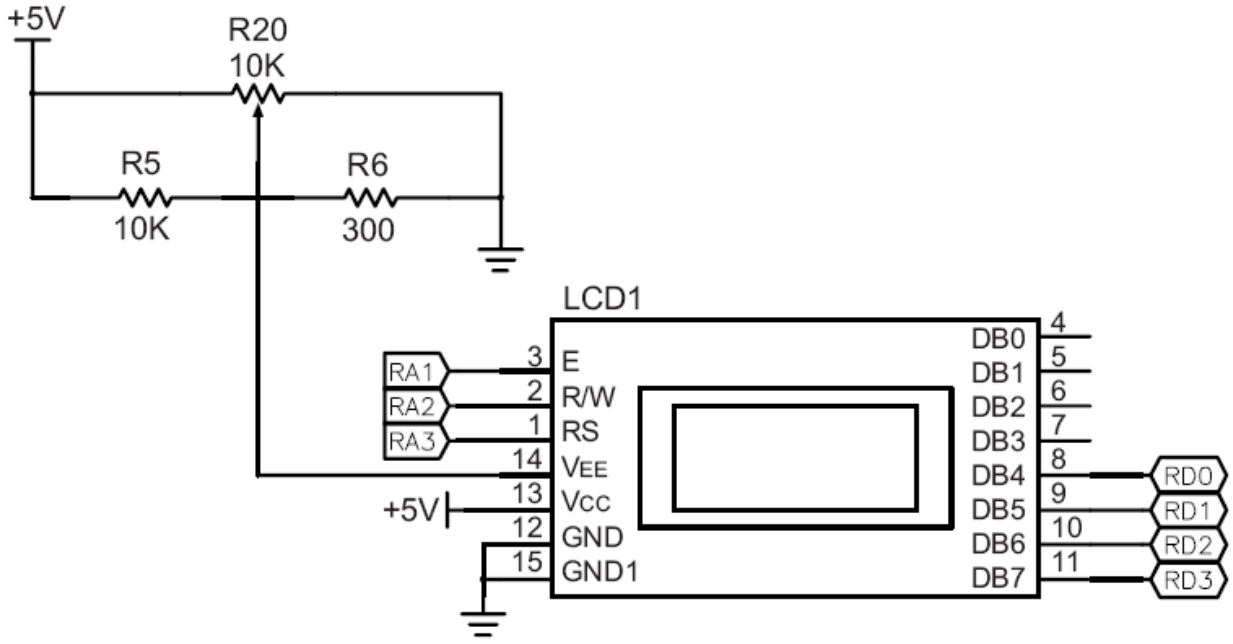
DOT MATRIX CHARACTER
LCD MODULE
USER'S MANUAL

Cliff notes

PicDem2 Plus connection to LCD



Standard Character Font Table

High order bit / Low order bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
X X X X0000	CG RAM (1)												
X X X X0001	(2)												
X X X X0010	(3)												
X X X X0011	(4)												
X X X X0100	(5)												
X X X X0101	(6)												
X X X X0110	(7)												
X X X X0111	(8)												
X X X X1000	(1)												
X X X X1001	(2)												
X X X X1010	(3)												
X X X X1011	(4)												
X X X X1100	(5)												
	(6)												
	(7)												
	(8)												

Data Display Memory Configuration

	Column															
	1	2	3	. . .	15	16	. . .	19	20	. . .	31	32	. . .	38	39	40
line 1	00	01	02		0E	0F		12	13		1E	1F		25	26	27
line 2	40	41	42		4E	4F		52	53		5E	5F		65	66	67

16 x 2

Table 1.4
Selection of Registers

RS	R/W	Operation
0	0	IR write, internal operation (Display Clear etc.)
0	1	Busy flag (DB_7) and Address Counter (DB_0 ~ DB_6) read
1	0	DR Write, Internal Operation (DR ~ DD RAM or CG RAM)
1	1	DR Read, Internal Operation (DD RAM or CG RAM)

4.2.1 Write Operation

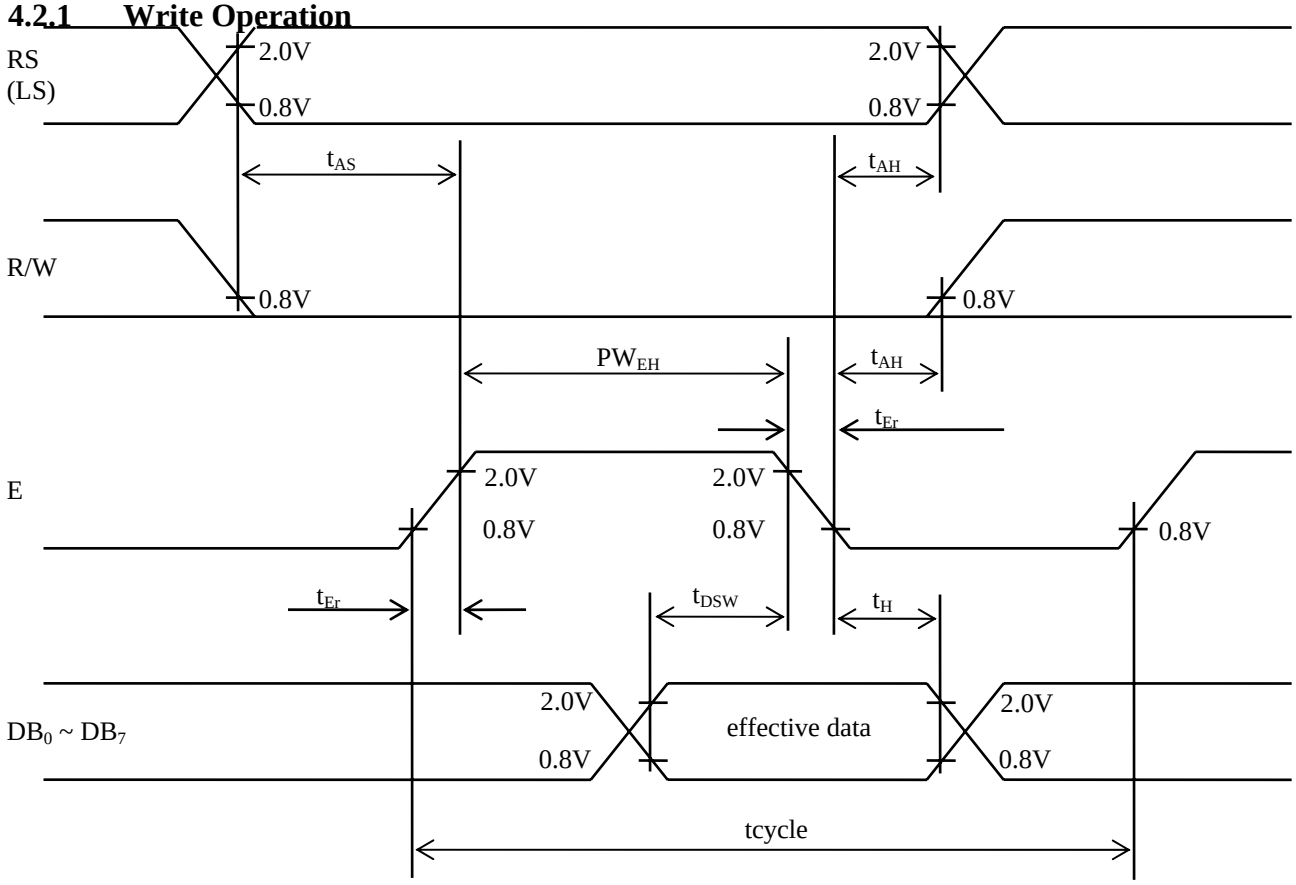


Fig. 4.1
Bus Write Operation Sequence.
(Writing data from MPU to Module)

4.2.3 Timing Characteristics of Each Drawing

(Vcc = 5.0V ± 5%, Vxx = 0V, Ta = 0 ~ 50↑C)

Write timing characteristics (Fig. 4.1)

Item		Symbol	Specs. Value		Unit
			Min.	Max.	
Enable cycle time		tcycle	1000	-	ns
Enable pulse width	"High" level	PW_{EH}	450	-	ns
Enable rising, falling time		t_{Er}, t_{Ef}	-	25	ns
Set up time	RS, R/W-E	t_{AS}	140	-	ns
Address hold time		t_{AH}	10	-	ns
Data set up time		t_{DSW}	195	-	ns
Data hold time		t_H	10	-	ns

Read timing characteristics (Fig. 4.2)

Item		Symbol	Specs. Value		Unit
			Min.	Max.	
Enable cycle time		tcycle	1000	-	ns
Enable pulse width	"High" level	PW_{EH}	450	-	ns
Enable rise, fall time		t_{Er}, t_{Ef}	-	25	ns
Set up time	RS, R/W-E	t_{AS}	140	-	ns
Data delay time		t_{DDR}	-	320	ns
Data hold time		t_H	20	-	ns

4.2.2 Read Operation

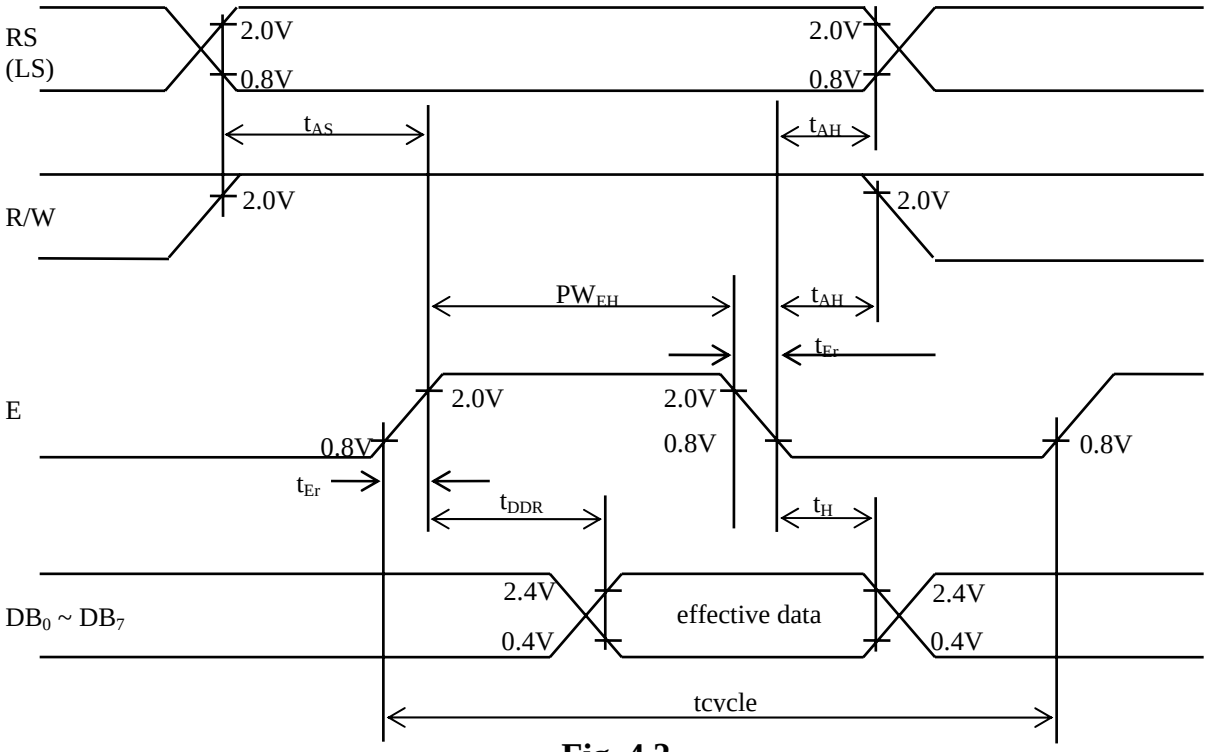


Fig. 4.2

Bus Read Operation Sequence
(Reading data from Module to MPU)

3.1.1 Clear Display

	RS	R/W	DB_7	DB_6	. . .			DB_1	DB_0
Code	0	0	0	0	0	0	0	0	1

Writes the space code "20" (hexadecimal) into all addresses of DD RAM. Returns display to its original position if it was shifted. In other words the display clears and the cursor or blink moves to the upper left edge of the display. The execution of clear display instruction sets entry mode to increment mode.

3.1.2 Return Home

	RS	R/W	DB_7	DB_6	. . .			DB_1	DB_0
Code	0	0	0	0	0	0	0	1	x

Sets the DD RAM address "0" in address counter. Return display to its original position if it was shifted. DD RAM contents do not change.

The cursor or the blink moves to the upper left edge of the display. Text on the display remains unchanged.

3.1.3 Entry mode set

	RS	S/W	DB_7	DB_6	. . .			DB_1	DB_0
Code	0	0	0	0	0	0	1	I/D	S

Sets the Increment/Decrement and Shift modes to the desired settings.

I/D: Increments (I/D = 1) or decrements (ID = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM.

The cursor or blink moves to the right when incremented by +1.

The same applies to writing and reading the CG RAM.

S: Shifts the entire display either to the right or to the left when S = 1; shift to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and only the display seems to move.

3.1.4 Display ON/OFF Control

	RS	R/W	DB_7	DB_6	. . .			DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

Controls the display ON/OFF status, Cursor ON/OFF and Cursor Blink function.

D: The display is ON when D = 1 and OFF when D = 0. When OFF due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0. The cursor is displayed on the 8^{th} line when 5 x 7 dot character font has been selected.

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all blank dots and display characters at 0.4 sec intervals.
The cursor and the blink can be set to display simultaneously.

3.1.6 Function Set

Sets the interface data length, the number of lines, and character font.

	RS	R/W	DB_7	DB_6	. . .			DB_1	DB_0
Code	0	0	0	0	1	DL	N	F	x	x

DL: Sets interface data length. Data is sent or received in 8-bit length (DB_7 ~ DB_0) when DL = "1", and in 4-bit length (DB_7 ~ DB_4) when DL = 0. When the 4-bit length is selected, data must be sent or received twice.
N: Sets the number of lines, N = "0":1 line display (1/8 duty), N = "1":2 line display (1/16 duty)
F: Sets character font. F = "1":5 x 10 dots, F = "0":5 x 7 dots

3.1.8 Set DD RAM Address

	RS	R/W	DB_7	DB_6	. . .	DB_1	DB_0
Code	0	0	1	A	A	A	A

← Higher order bits Lower order bits →

Sets the address counter to the DD RAM address AAAAAAA. Data is then written/read to from the DD RAM.

For a 1-line display module AAAAAAA is "00" ~ "4F" (hexadecimal). For 2-line display module AAAAAAA is "00" ~ "27" (hexadecimal) for the first line and "40" ~ "67" (hexadecimal) for the second line. (See section 1.7.6 "DD RAM addressing")

3.1.10 Write Data to CG or DD RAM

	RS	R/W	DB_7	DB_6	. . .	DB_1	DB_0
Code	1	0	D	D	D	D	D

← Higher order bits Lower order bits →

Writes binary 8-bit data DDDDDDDD to the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be written (CG RAM address set or DD RAM address set). After a write the entry mode will automatically increase or decrease the address by 1. Display shift will also follow the entry mode.

1.7.5 Address Counter (AC)

The DD RAM address (ADD) is set in the Address Counter (AC) and is represented in hexadecimal notation.

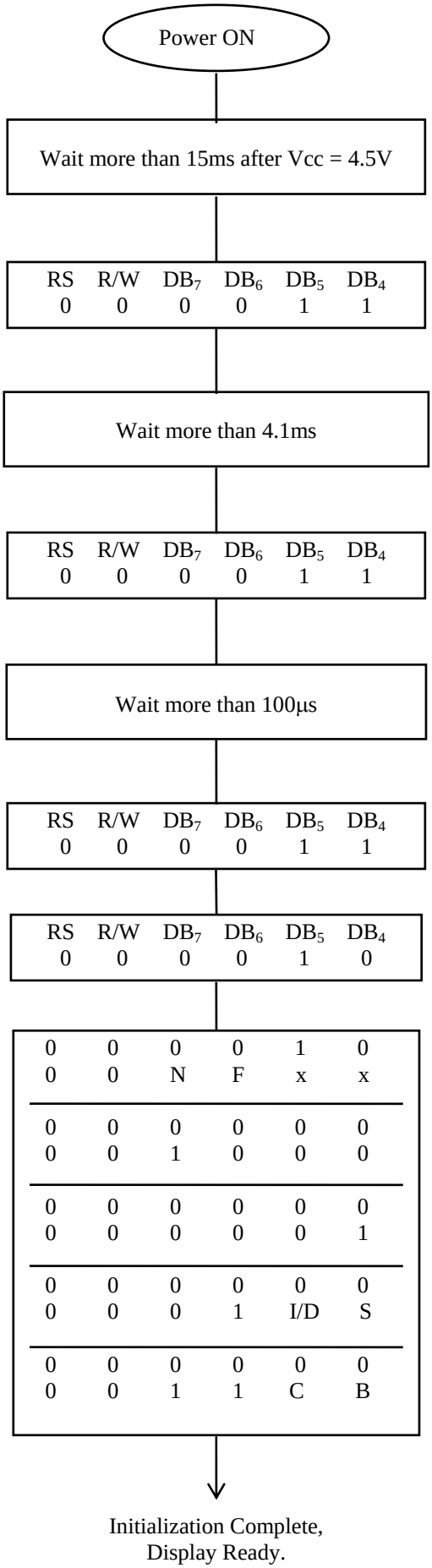
The address counter can be written using the "Set DD RAM Address" instruction and can be read using the "Read Busy Flag and Address" instruction. In each case, data bits D_0-D_6 represent the DD RAM address. In the read operation, bit D_7 represents the "Busy Flag".

	MSB							LSB
AC:	BF	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
	Busy Flag	Hexadecimal			Hexadecimal			

Example 1DD RAM address "4E"

BF	1	0	0	1	1	1	0
Busy Flag		4			E		

2.2.2.2 4 - Bit Initialization:



No data should be transferred to or from the display during this time.

Function Set Command: (8-Bit interface)

No data should be transferred to or from the display during this time.

Function Set Command: (8-Bit interface)

No data should be transferred to or from the display during this time.

Function Set Command: (8-Bit interface)
After this command is written, BF can be checked.

Function Set: Sets interface to 4 -bit

Function Set (Interface = 4 -bit, Set N and F for number of lines and character font)

Display OFF

Clear Display

Entry Mode Set:

Display ON (Set C and B for cursor/Blink options.)

Note: Delays are required between three consecutive "Function Sets." See table 3.1 next page

Note: BF should be checked before each of the instructions starting with Display OFF.

Table 3.1
List of Instructions

Instruction	Code										Description	Execution time (max.) when fcp or fosc is 250 kHz
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	15.2ms
Return Home	0	0	0	0	0	0	0	0	1	x	Sets DD RAM address 0 in address counter. Also returns shifted display to original position. DD RAM contents remain unchanged.	15.2ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift or display. These operations are performed during data write and read.	40μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Moves cursor and shifts display without changing DD RAM contents.	40μs
Function Set	0	0	0	0	1	DL	N	F	x	x	Sets interface data length (DL), number of display lines (N) and character font (F).	40μs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40μs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	40μs
Read Busy Flag & Address	0	1	BF	AC							Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40μs
	I/D=1 : Increment I/D=0 : Decrement S=1 : Accompanies display shift S/C=1 : Display shift S/C=0 : Cursor move R/L=1 : Shift to the right R/L=0 : Shifts to the left DL=1 : 8 bits, DL=0 : 4 bits N=1 : 2 lines, N=0 : 1 line F=1 : 5x10 dots, F=0 : 5x7 dots BF=1 : Internally operating BF=0 : Can accept instruction										DD RAM : Display Data RAM CG RAM : Character Generator RAM ACG : CG RAM address ADD : DD RAM address. Corresponds to cursor address. AC : Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes. Example: When fcp or fosc is 270kHz: 40μs x 250/270 = 37 μs

x = don't care. (No Effect)